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Logic Circuit Design Using Feedback Equalization Technique

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ABSTRACT: Low energy or low power are the primary constraints in the design of digital VLSI circuits in recent years. Minimum-energy consumption can be achieved in digital circuits by operating it in the sub-threshold region. However, this regime can only be achieved by proper body-biasing and transistor up-sizing. Slow speed is a main drawback which can have a detrimental impact on the functionality of the circuits operating under lower supply voltages. This becomes more frequent in scaled technology nodes where process variations are highly prevalent. Therefore, mechanisms to mitigate these timing errors in circuits are required. The proposal in this paper is to use a Variable threshold feedback equalizer circuit with combinational logic blocks to mitigate timing constraints, which can then be leveraged to reduce the propagation delay. As part of the analysis, a conventional D Flip flop is compared with a proposed Equalized flip flop. The power and delay analysis of these circuits are done in Cadence tool. It is found that in 180 nm technology, the equalization technique has 10.97% lower propagation delay than the non-equalized logic design.

KEYWORDS: Sub-threshold logic, Transmission gate, D flip-flop, VTI, CADENCE Virtuoso tool.

I. INTRODUCTION

This is the era in which technology scaling is at its highest hits. The major constraint in the design of a VLSI circuit is low energy or low power. The performance of a circuit in terms of power and speed are of particular interest. As the technology gets scaled down, it affects the voltage being supplied and size of the transistor used [2]. And supply voltage is scaling down in such a way that the circuit is forced to work in sub threshold regime [3]. Sub-threshold conduction occurs for gate to source voltages (Vgs) below the threshold voltage (Vth).

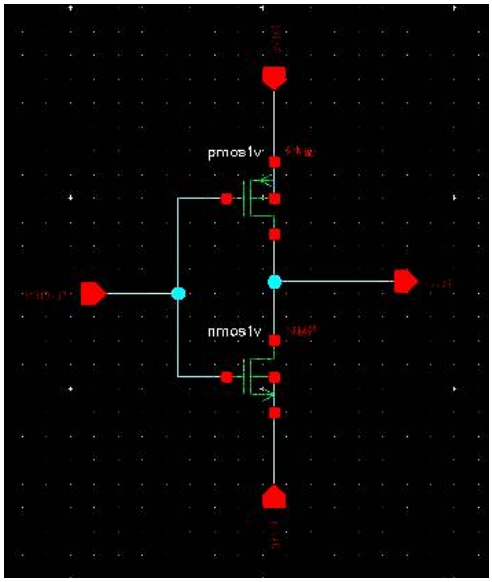

Fig. 1: Schematic of an Inverter

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Fig 1 shows the schematic of an inverter in 180 nm. Supply voltage is scaled down from 1.8 V to 500 mV. Upto 600 mV perfect inverted output was obtained. But for 500 mV supply, that was not the result. In order to obtain perfect operation as an inverter, it required various techniques viz., body biasing [6] and upsizing the transistor. Standard configuration has the bulk of the NMOS tied to the ground terminal, while that of the PMOS is tied to the power supply (VDD) for an inverter. If the bulk terminal [7] of the NMOS device is raised above ground and the power supply voltage is below the threshold, there is increase of the drain current (I_D).Lowering the bulk voltage of pmos device leads to increased ID. In this case transistor Vgs is found out to be less than it's Vth which is the threshold voltage. And thus circuit operates in sub-threshold region [1].

Table 1: Voltage Scaling Effects

V_{DD}	Power(µW)	Delay(ns)	Wp:Wn	Body-bias
1.8 V	46.4	9.865	2:1	NO
900 mV	0.5	10.027	2:1	NO
600 mV	0.267	10.264	2:1	NO
500 mV	0.204	11.581	5:1	YES

In all these cases, the dynamic power and propagation delay [9] were found out. From Table1, we can observe that as voltage gets scaled down [3], the power is reducing, as dynamic power is proportional to the square of supply voltage. But propagation delay is increasing when voltage scales down. So in order to operate my device in scaled [8] technology nodes the main problem is higher propagation delay or slow speed [4].This paper mainly deals with a feedback equalization circuit using variable threshold inverter to improve speed than non-equalized one. The rest of the paper is organized as follows. Section II discusses the working of a variable threshold inverter. A detailed description of the operation of the conventional D-flip flop circuit is presented in Section III. In Section IV, we discuss the proposed feedback equalizer circuit to reduce the propagation delay. Section V discusses the effect of technology scaling on the propagation delay using the feedback equalizer circuit and non-equalized circuit followed by concluding remarks in Section VI.

II. VARIABLE THRESHOLD INVETER

Variable threshold inverter [12] is a circuit that adjusts the switching thresholds and mitigates timing errors.

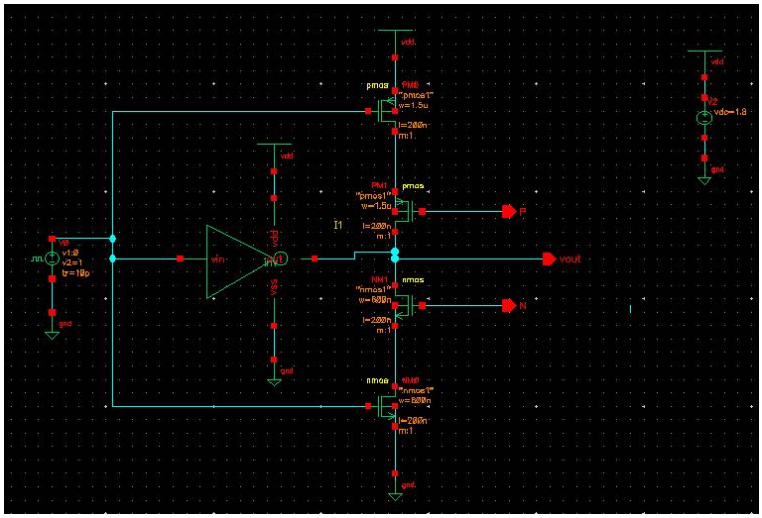

Fig. 2: Schematic of a Variable Threshold Inverter (VTI)

The VTI [10] circuit shown in Fig.2 is analyzed in 180 nm process. Switching threshold voltage is found out to be greater than or less than nominal threshold voltage. Table 2 shows the values obtained for various values of P and N control signals.

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Variable threshold inverter fastens the transition from low-to high and high-to-low. The threshold voltage of the inverter is controlled by using signals P and N. When P is grounded and N is connected to VDD, the threshold voltage is V th0, which is the nominal threshold voltage of the inverter. When both P and N are grounded, the pull down path is off and the threshold voltage increases to V th^+. Similarly, when both P and N are connected to VDD, the pull up path is off and threshold voltage decreases to V th^-. A weak inverter is required in this case, to ensure that the output of the inverter is never floating.

Table 2: Switching Threshold of VTI

P	N	V_M (mV)	V_{th}
V_{DD}	V_{DD}	734.198	V_{th}^-
GND	V_{DD}	826.047	V_{th}^0
GND	GND	938.476	V_{th}^+

III. THE CONVENTIONAL D FLIP-FLOP

The working of D flip flop [5] is similar to the D latch with one exception. The exception is that the output of D Flip Flop (D-FF) takes the state of the D input at the moment of a positive edge at the clock and delays it by exactly one clock cycle. That's why, it is commonly known as delay flip flop. D-FF can be interpreted as a delay line or zero order hold. The advantage of the D-FF over the D type "transparent latch" is that the signal on the D input pin is captured the moment the flip flop is clocked, and subsequent changes on the D input will be ignored until the next clock event. Transmission gates are used in the construction of Master Slave flip flop shown in Fig.3.

Transmission gate is constructed using PMOS and NMOS which are actually tiled face to face. The Master Slave(MS) flip flop[13] consists of cascading a master stage with a slave stage. When clock is low, the master stage is transparent and the D input is passed to the master stage output, QM and the slave stage is in the hold mode, which keeps its previous value using feedback circuit.

On the rising edge of the clock, the slave stage starts sampling whereas master slave stops sampling. During high phase of the clock, the master stage remains in hold mode, while the slave stage samples the output of the master stage (QM). Since Q_M is constant during the high phase of the clock, Q makes only one transition per cycle. The value of Q is the value of D right before the rising edge of the clock, achieving the positive edge-triggered effect. A negative edge-triggered register can be constructed with same principle as that of a positive edge-triggered flip flop, but by switching the order of the positive and negative latch (i.e., by placing the positive latch first).

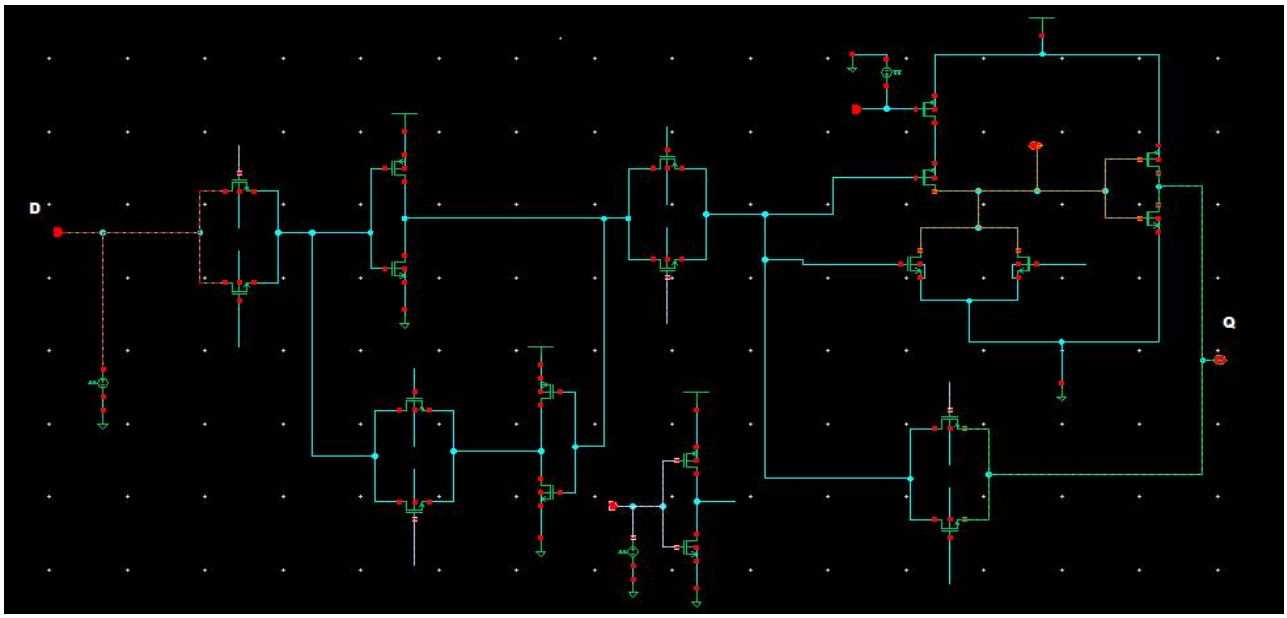

Fig. 3: Schematic of a D Flip-Flop

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IV. THE PROPOSED EQUALIZED FLIP-FLOP

The proposal is to use a feedback equalizer circuit [13] in the design of logic circuits operating in lower supply voltages. This feedback equalizer circuit takes the advantage of fast charging/ discharging of the load capacitance in the critical path, which creates opportunities for voltage scaling. The use of the feedback equalizer[14] circuit in the design of an equalized flip flop and then provide a detailed comparison of the equalized flip flop with a conventional flip flop in terms of area, power and performance. We propose the application of a feedback equalizer (designed using a variable threshold inverter shown in Figure 2) along with the classic master-slave positive edge triggered flip flop to implement an equalized flip flop. The equalized flip flop [14] shown in Fig.4, dynamically modifies the switching threshold of the gate before the flip flop based on the previous sampled data. If the previous output of the gate is a zero, the equalized flip flop lowers down the switching threshold which speeds up the transition to one. Similarly, if the previous output is one, the equalized flip flop increases the switching threshold which speeds up the transition to zero. In this configuration, the circuit adjusts the switching threshold and facilitates faster high-to-low and low-to-high transitions. The switching of the variable threshold inverter is dynamically adjusted based on the previous sampled output data.

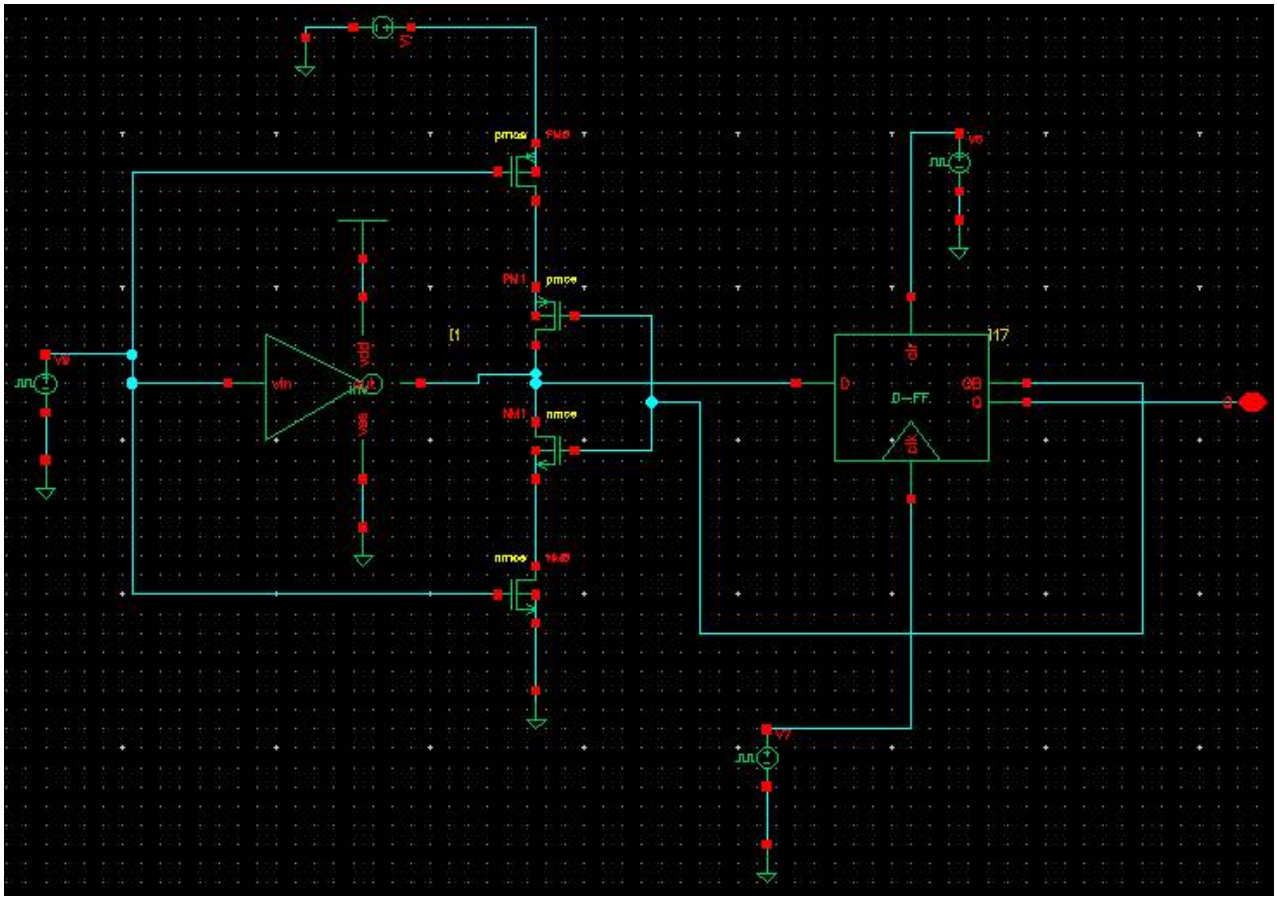

Fig. 4: Schematic of an Equalized flip-flop

V. SIMULATION RESULTS

The analyses of equalized flip flop and non-equalized flip flop in 180 nm process are compared. For the same combinational logic output, which is here taken as a pulse input both the circuits exhibits different results. On an average, the equalization technique (Table3) has 10.97% lower propagation delay than the non-equalized logic design. But the power dissipation of an equalized circuit is 5.06% more than that of its non-equalized version. This extra power

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is caused by the extra circuitry used for feedback equalization. Power delay product (Table4) of an equalized circuit is 7.81% less than non-equalized one.

Table 3: Comparison of NE circuit versus E circuit

V_{DD}	Delay of NE ckt (ns)	Delay of E ckt (ns)	P_{NE}(mW)	P_E(mW)
1.8 V	25.6	24.1	121	123.1
900 mV	32.57	28.2	105.6	111.37
600 mV	33.645	29.1	92.54	100.1

Table 4: Power Delay Product (PDP) of NE versus E circuit

V_{DD}	PDP of NE ckt (nJ)	PDP of E ckt (nJ)
1.8 V	3.1	2.9
900 mV	3.4	3.1
600 mV	3.1	2.9

VI. CONCLUSION

The analyses done on the conventional D flip flop and Equalized flip flop is compared. It is found that there is a noticeable decrement in the propagation delay of the equalized flip-flop than its non-equalized version (Fig.5).

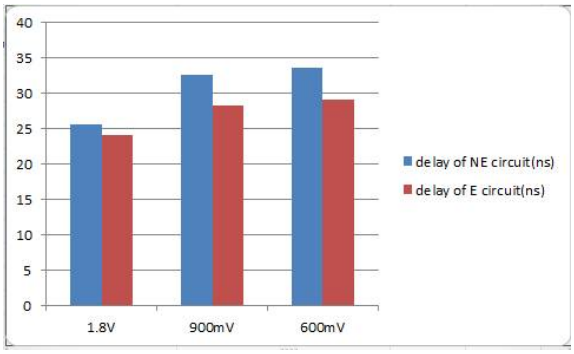

Fig. 5: Supply voltage versus delay of Non-equalized and Equalized circuit

But the power of Equalized flip flop is more than that of non-equalized flip flop. This is due to the fact that Feedback equalization circuit which consist of a Variable threshold inverter is having an area overhead of 27%. These added 6 transistors
in VTI circuit adjust the switching threshold and speeds up the operation. The analyses also emphasize on the fact that good speed can be maintained at a scaled voltage with this feedback equalization circuit. The power delay product (PDP) calculated as per the analyses results also shows an optimized output. PDP of Equalized (E-ckt)circuit is less than that of Non-equalized (NE-ckt) circuit.

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